Single-Event Upset Test Results for the Xilinx R1701L PROM

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SUMMARY

Radiation testing of the Xilinx R1701L 3.3V 1-Mb serial PROM took place on September 14 and 15, 1999 at SEE Test Facility, Brookhaven National Lab. The R1701L is a special version of the standard commercial XQ1701L PROM that is fabricated on an epitaxial substrate, 7μm thick, in order to reduce susceptibility to latchup. The data taken here is similar to that taken for the 1999 NSREC workshop publication on the standard XQ17011 part which uses a bulk substrate [1]. Latchup was not observed in the R1701L part up to LET=120 MeV cm^2/mg (σ_{LU}<5x10^{-8}cm^2), indicating that the processing change was successful in improving the latchup hardness of the device. It is important to note, however, that latchup may not be the greatest concern for this device, depending on the application, because the special version of the part is still susceptible to single-event upset effects. Careful consideration must be given when using these devices for space applications to allow for the various single event upset effects and their impact on FPGA devices that are interfaced to the PROM.

INTRODUCTION

Programmable logic devices are frequently used in space applications because of the ease of reconfiguration which significantly lowers overall cost. Earlier work has been done to investigate the effects of radiation on some of these technologies [2-8], most of which use antifuse technology for programming. The SRAM-configurable Xilinx gate arrays require an initial programming sequence on power-up in order to set up the internal SRAM contents. This report presents test results for a special version of a 3.3-V 1-Mbit serial PROM that is designed to interface with Xilinx FPGAs (field programmable gate arrays) and provide the initialization sequence.

The R1701L is a one-time programmable read-only memory with a serial output. It provides the same functionality as the standard commercial XQ1701L except that the R1701L is made on a highly doped substrate with a 7 μm epitaxial layer on the surface; the epitaxial substrate reduces latchup susceptibility but does not otherwise affect the operation of the device. These devices are compatible with the configuration requirements of a number of 3.3-V Xilinx XC4000 and 2.5-V Virtex FPGAs which are attractive to spacecraft designers. The configuration memory in these FPGAs that is loaded by the PROM is SEU susceptible [4-6]. The threshold LET was approximately 5 MeV-cm^2/mg for the tested 5-V [4] and 3.3-V [5] FPGAs. This is a relatively low threshold level, and it is generally necessary to use repetitive reconfiguration (or other system approaches) in order to deal with the prospect of FPGA errors induced by radiation. These FPGAs do appear suited to a broad range of other applications, such as sensor and camera controllers.

Xilinx has used special processing to produce special versions of a number of their FPGAs with a 7μm epitaxial layer in ceramic packages. They market these devices as high reliability, radiation tolerant devices [9]. The "radiation tolerant" claim is based on the fact that latchup, which occurs in their standard part, does not occur on the devices with special processing along with the capability of continually monitoring the configuration SRAM for upsets. The special processing does not affect total dose hardness, which is adequate for many applications with the standard commercial part. Single-event upset, which is not significantly changed by the processing change, remains a potential issue for the special versions of these devices.

Because re-loading the FPGA takes a large fraction of a second, designs for collecting critical data or controlling expendables require a significant risk mitigation effort. The PROM is critical for these applications, because any errors in the PROM will cause erroneous configuration of the FPGAs with which it interfaces. Like the "radiation tolerant" FPGAs, however, the PROM has similar upset susceptibility with a threshold near 5 MeV-cm^2/mg. The upset types seen in the 7 μm-epi R1701L are an erroneous end-of-pass signal, an address upset, and a low power mode called "stuck at 0" because the output always registers a logical 0 with the test equipment used.

TEST DEVICE PREPARATION

Five samples of the R1701L PROM were delidded and serialized as x4092, x4093, x4094, x4095, and x4096. The devices were mounted on daughter boards designed to allow the 44-pin LC44 package to mate with ZIF sockets. All parts programmed, but most required re-seating in the programming socket several times before they blank-checked successfully prior to programming (average re-seats/part:3).

During testing only three devices. -- x4093, x4094, and x4095 -- were used. Several standard parts (bulk substrate) were prepared and included in the tests to check on consistency with earlier results; those results closely match the previously reported data [1] and are not discussed further in this report.

TEST CODE PREPARATION

The devices were programmed using a Xilinx HW130 programmer with a pattern that was approximately half "ones" and half "zeros". It was designed to permit trapping of selected types of errors. An actual configuration pattern was not used. The pattern used was selected in order to gain visibility on selected types of errors during dynamic testing.

Initially, two different algorithms were used to capture upset events and categorize them. The first, simpler, algorithm began by resetting the part, and then applying a sequence of clock signals. With this algorithm, no attempt was made to compare the output of the memory. Error detection was based on detection of the end-of-address-space output (CEO pin), ensuring that it only provided an output at the end of the proper number of clock cycles. If the CEO output occurred prematurely or failed to occur when expected, that indicated an error had occurred in the address control logic. The advantage of this algorithm was ease of execution. It was primarily used for initial evaluations of the devices to determine what types of errors and malfunctions occurred.

A second, more sophisticated algorithm was used to accomplish a more complete test of the parts. That algorithm executed a bit-by-bit comparison of the actual output from the PROM to the correct (or expected) value. The pattern included a "marker" that the address was encoded into, partitioning the device into identifiable 32-bit sections. Each section held the marker and its own address. Upon reading 32 bits, the test algorithm attempted to find the marker. If it did, it compared the embedded address with the last known location. A difference between the last read location and the current location indicated an address error.

With this algorithm, error visibility depends on error rate. If errors occur too fast, there were more misidentifications which tended to undercount actual errors. Getting out of synchronization with the serial data stream also meant it was possible to see more bits apparently in error than actually were in error. Under this coding scheme and the beam fluxes used, the rate of address errors is estimated to be within 5% of the actual rate.

Finally, a modified version of the second algorithm was implemented to more accurately identify all address errors. The difficulties in the previous attempts at making the algorithm bullet-proof suggested tracking the information as it was read from the device. The program was modified to automatically log the entire data stream on a run-by-run basis. The test algorithm was also modified to determine the actual amount of time spent in the functional interrupt (SEFI) low current mode known as "stuck at 0." Several other functionality and efficiency issues were also improved in the revised program.

OBSERVATIONS ON BEHAVIOR

For these tests there were five possible error modes: latchup, bit stream error, address failure, end-of-pass assertion failure, and SEFI. Of these, the last three were seen in the R1701L testing. Single-event

latchup was not seen with a total fluence of $2x10^7/cm^2$ ions at LET = 120 MeV cm^2/mg. No clearly identifiable bit-stream errors were seen, and the cross-section was less than $5x10^{-6}$ cm^2/device.

The first error mode seen in this testing was address failure. Most of the time this appeared to result from a single bit upset in the internal address register (or counter). However, a significant fraction (~40%) of address errors are a reset (to zero) of the address register. Occasionally, two or more bits of the address register were upset; this appears to be consistent with Poisson statistics.

The second error mode observed was the end-of-part (EOP) assertion failure. An EOP error is constituted by a discrepancy between the end of data indicated by the device pin and the actual known end of data as verified by address location. Virtually all end-of-part failures were an assertion of the end of part pin when the data stream was reading out from other parts of the device.

The third and most important error seen on this hardened version of the device was low current functionality interrupt or SEFI, designated as "*stuck at 0*" because the output apparently hangs low. Two features of this mode are the apparent continued operation of the internal address register, and the occasional logical high reading at the output pin. The first feature suggests that this interrupt may only be turning off the output pin. The second seems to confirm this. It seems likely that the output pin is being tri-stated and that the occasional high output value may be related to the transition level of the device reading the pin.

EXPERIMENTAL RESULTS

The most significant result of this testing was that the 7 μm epitaxial layer was effective in reducing latchup susceptibility. No latchup events were observed, even with an LET of 120 MeV-cm^2/mg (with a fluence of $2x10^7$ particles/cm^2). However, even though this version of this device did not show latchup, the information below shows that these devices have single-event upset behavior that is similar to (though somewhat worse than) that of the unhardened commercial parts.

Data for the three detected SEU effects are shown in figures 1 , 2, and 3 on the following pages. Figure 1 shows the cross section vs. LET response for the "EOP fail" effect (incorrectly asserted end-of-pass signal). Figure 2 shows the cross section vs. LET response for the "Address Fail" effect (partial and total address reset as well as single-event bit-upset in the address holding register). Figure 3 shows the cross section vs. LET response for the "Stuck at 0" effect (the device drops to a low current state where the data output always responds low. All of the data for these figures is presented in the appendix, along with the number of bit stream errors. The numbers in the Bit column in the appendix are probably not bit stream errors, but are more likely evidence of a testing artifact where the program doesn't catch address errors exactly when they happen.

It should be noted that the error bars shown on the figures are 2-σ values, based on upsets being a Poisson random variable. For large numbers of events, the error bars show twice the square root of the number of events. The fitted curves are diffusion, based after Edmonds [10].

DISCUSSION

The improved latchup results clearly favor the selection of the R1701L over its commercial counterpart (the XQ1701L). However, the susceptibility of the R1710L to single-event upset is essentially the same for the two different device types. For the R1710L, upsets were detected that caused errors in the address-fail mode and the "*Stuck at 0*" mode. The threshold LET for both upset modes was about 3.5 MeV-cm^2/mg, which is very low. In addition to upsets from heavy ions, the low upset threshold makes it nearly certain that these devices will upset when they are exposed to high-energy protons as well as heavy ion (other devices have been sensitive to proton upset when the LET threshold was below approximately 10 MeV-cm^2/mg). The error rates discussed later do not consider upset from protons, which would not only increase the upset rate during "quiet" periods but would also make these devices far more sensitive to upset during a solar flare.

The error modes caused by single-event upset do not cause catastrophic failure, but the internal architecture of these devices causes these internal errors to remain until specific steps are taken to return the device to normal operating conditions. There are only two ways of getting out of the "*Stuck at 0*"

SEFI: power cycle the device, or hope that it will upset itself out of the mode (very unlikely in practice because the likelihood of a second event that fortuitously cancels the first event is extremely low). Note that both resetting the device and/or disabling the chip will *not* allow it to recover from this type of internal logic failure condition.

The accuracy of cross section data is affected by the number of events that are observed during a test run because of statistical counting uncertainties. The uncertainty in cross section is typically 20% or better, and is within about 50% even for cases where fewer events were observed. Using a standard galactic cosmic ray (GCR) model, the probability of a functional error during solar maximum GCR is estimated to be 3.0% per device-year of operation (see table 1). Calculations were also done using the solar flare heavy ion model (at 1 AU and behind 100 mil aluminum shield) developed by JPL. The probability of a functional error from such a flare, given that one occurs, is calculated to be 19% (these rates are higher than reported for the commercial XQ1701L due to the slightly lower threshold LET [1]). Note these are heavy ion rates; proton errors may be more frequent in some environments.

Table 1. Upset rates for the R1701L – behind 100 mils of aluminum shielding

Upset Type	Solar Minimum GCR (upsets/device-year)	Solar Flare Heavy Ion Model (upsets/device-flare)
End of Pass Fail	3.6×10^{-3}	1.9×10^{-2}
Address Fail	2.9×10^{-2}	1.5×10^{-1}
Stuck @ 0	2.8×10^{-3}	1.3×10^{-2}

CONCLUSIONS

The Xilinx R1701L does not show a latchup problem up to an LET of 120 with 1×10^{7} ions. However, designers must provide a mitigation method to recover from the "Stuck @ 0" SEFI mode because the device cannot recover on its own without a fortuitous (and unlikely) upset that reverses the error. Power cycling the device is required to resume normal operation.

Other upset modes may preclude the use of the R1701L in monitoring schemes designed to protect FPGAs from SEUs in the configuration SRAM. It is important to evaluate whether or not the PROM error rates make continuous monitoring useful. While the R1701L's resistance to latchup is a strong positive factor, design challenges remain for spaceflight application of the device.

REFERENCES

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Appendix

Topping the columns in the collected data table in the appendix are a few headings whose meanings may not be immediately obvious. Several notes:

- Flux, Fluence, Angle, effective LET, and Range are measured in particles per cm^2 per second, Flux times time, degrees, MeV-cm^2/mg, and μm respectively.
- "%Bad" represents the fraction of the time the device was not driving the output line (e.g. when it was "Stuck @ 0").
- "Bit", "Addr", "EOP", "S@0", and Reset refer to observed events during the test; bit errors, address fails, EOP fails, "Stuck @ 0"'s, and partial address resets respectively.
- The "U" column represents the number of times the collection program was unable to determine what the part was doing. For the most part "U"s occurred in strings following unexpected logical highs during the "Stuck @ 0" SEFI mode.

Run#	Serial#	Flux	Fluence	Ion	Angle	effective LET	Range	%Bad	Bit	Addr	EOP	S@0	U
14	x4093	4.29E+04	1.00E+07	Ni-58	0	26.6	42.4	24	0	77	7	8	7
15	x4093	3.16E+04	9.92E+06	Ni-58	45	37.6	30	18	0	102	8	10	9
16	x4093	2.34E+04	1.00E+07	Ni-58	60	53.1	21.2	22	1	148	10	17	106
17	x4094	5.58E+04	1.00E+07	Ni-58	0	26.6	42.4	21	2	69	5	8	0
18	x4094	3.83E+04	1.00E+07	Ni-58	45	37.6	30	15	2	120	7	7	8
19	x4094	2.72E+04	1.01E+07	Ni-58	60	53.1	21.2	37	1	107	21	15	8
20	x4095	5.50E+04	1.00E+07	Ni-58	0	26.6	42.4	17	0	66	9	9	11
21	x4095	3.89E+04	1.00E+07	Ni-58	45	37.6	30	19	1	98	12	9	9
22	x4095	2.55E+04	1.00E+07	Ni-58	60	53.1	21.2	30	1	153	12	18	18
88	x4093	2.99E+04	1.17E+07	Br-81	0	37.3	36.7	21	0	131	8	14	418
89	x4093	2.15E+04	5.01E+06	Br-81	45	52.8	25.9	21	0	75	10	8	8
90	x4093	1.55E+04	5.01E+06	Br-81	60	74.7	18.3	36	0	65	11	11	7
91	x4094	3.04E+04	5.01E+06	Br-81	0	37.3	36.7	31	0	42	6	6	3299
99	x4094	1.24E+05	2.01E+07	I-127	0	59.9	32.7	22	0	238	29	30	278
100	x4093	1.74E+05	2.01E+07	I-127	0	59.9	32.7	36	2	222	33	29	152
101	x4093	1.24E+05	2.01E+07	I-127	45	84.7	23.1	32	5	305	37	47	459
102	x4093	5.44E+04	2.00E+07	I-127	60	120	16.4	47	1	317	43	66	187
103	x4093	1.82E+05	2.15E+07	Cl-35	0	11.4	63.5	41	0	26	4	4	0
104	x4093	1.25E+05	2.00E+07	Cl-35	45	16.2	44.9	51	1	58	9	6	2
105	x4093	8.69E+04	2.00E+07	Cl-35	60	22.9	31.7	50	2	75	6	13	200
106	x4094	1.72E+05	2.01E+07	Cl-35	0	11.4	63.5	41	0	26	4	4	3
111	x4093	6.66E+04	2.00E+07	Cl-35	66.5	28.7	25.3	37	3	95	20	13	1988
112	x4093	2.83E+05	2.13E+07	Mg-24	0	6.26	75.9	4	0	25	3	1	1
113	x4094	2.98E+05	2.02E+07	Mg-24	0	6.26	75.9	27	0	21	2	2	0
114	x4093	1.95E+05	2.00E+07	Mg-24	45	8.85	53.7	69	0	20	2	4	3
115	x4093	1.22E+05	2.00E+07	Mg-24	60	12.5	38	55	0	2	7	9	7
123	x4093	1.61E+05	2.01E+07	F-19	0	3.36	122	31	0	1	0	1	0
124	x4093	1.36E+05	2.01E+07	F-19	30	3.88	105	62	0	1	0	1	0
125	x4093	1.09E+05	2.01E+07	F-19	45	4.76	86.1	0	0	0	0	0	0
126	x4093	7.61E+04	2.00E+07	F-19	60	6.73	60.9	93	0	0	0	1	0
127	x4093	7.67E+04	2.00E+07	F-19	60	6.73	60.9	0	0	1	0	0	0

Additionally, during this testing, more data was taken on the non-epi XQ1701L commercial part. A table of the results from that testing, using the same test methods is included here:

Run#	Serial#	Flux	Fluence	Ion	Angle	effective LET	Range	%Bad	Bit	Addr	EOP	S@0	U
8	x4088	4.46E+04	5.01E+06	Ni-58	0	26.6	42.4	23	0	32	4	3	2
9	x4088	3.17E+04	1.00E+07	Ni-58	45	37.6	30	20	0	85	11	7	352
10	x4088	2.40E+04	1.00E+07	Ni-58	60	53.1	21.2	61	1	43	12	14	6916
11	x4089	4.54E+04	1.00E+07	Ni-58	0	26.6	42.4	55	1	43	7	5	1
12	x4089	3.32E+04	1.00E+07	Ni-58	45	37.6	30	47	0	51	12	9	6
13	x4089	2.29E+04	9.94E+06	Ni-58	60	53.1	21.2	57	1	66	31	29	1066
92	x4088	3.04E+04	5.01E+06	Br-81	0	37.3	36.7	41	0	26	6	3	1
93	x4088	2.20E+04	5.14E+06	Br-81	45	52.8	25.9	63	0	21	33	10	1928
94	x4088	1.54E+04	5.01E+06	Br-81	60	74.7	18.3	59	0	29	83	18	3841
95	x4088	5.84E+04	2.00E+07	Br-81	60	74.7	18.3	70	0	58	244	57	2241
96	x4088	1.84E+05	2.15E+07	I-127	0	59.9	32.7	66	1	40	172	42	860
97	x4088	1.27E+05	2.02E+07	I-127	45	84.7	23.1	47	3	49	364	63	858
98	x4088	8.78E+04	2.00E+07	I-127	60	120	16.4	56	6	27	520	84	2258
107	x4088	1.72E+05	2.01E+07	Cl-35	0	11.4	63.5	20	0	45	5	2	2
108	x4088	1.21E+05	2.01E+07	Cl-35	45	16.2	44.9	47	2	48	5	4	3
109	x4088	8.40E+04	2.00E+07	Cl-35	60	22.9	31.7	58	0	9	8	4	11789
110	x4088	6.70E+04	2.00E+07	Cl-35	66.5	28.7	25.3	62	1	56	5	5	6
116	x4088	2.00E+05	2.01E+07	Mg-24	0	6.26	75.9	26	0	16	1	1	0
117	x4088	1.19E+05	2.00E+07	Mg-24	45	8.85	53.7	27	0	31	3	2	2
118	x4088	8.48E+04	2.00E+07	Mg-24	60	12.5	38	58	0	31	3	2	1
119	x4088	2.27E+05	2.16E+07	F-19	0	3.36	122	0	0	0	0	0	0
120	x4088	1.41E+05	2.02E+07	F-19	45	4.76	86.1	0	0	0	0	0	0
121	x4088	1.07E+05	2.01E+07	F-19	54	5.72	71.5	0	0	0	0	0	0
122	x4088	8.43E+04	2.00E+07	F-19	60	6.73	60.9	0	0	6	0	0	0